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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/700,520	11/05/2003	Le-Trong Nguyen	SP015.C18	5916

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EXAMINER	
PAN, DANIEL H	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 10/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/700,520	NGUYEN ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-44,46,48 and 50* is/are rejected.

7)☒ Claim(s) *45,47,49 and 51* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

11/05/03

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 08/30/04, 03/29/04, 02/19/04, 01/23/04, 01/09/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 8-52 are presented for examination. Claims 1-7 have been canceled.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 8, 14 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 29 of U.S. Patent No. 6,647,485. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons :

3. Although the patented claim 29 did not recite a bus connected between the memory and the processor as in current claims 8,14, it would have been obvious to one of ordinary skill in the art to use the a bus connected between the memory and processor because the patent claim 29 already taught the processor included data routing path between the functional units and configured to transfer data, therefore, one of ordinary skill in the art should be able recognize the use of a bus between a memory and the processor in the system for the purpose of transferring

the data , furthermore, claims 18,14 are generic to the species of invention covered by claim 29 of the patent. Thus, the generic invention is "anticipated" by the species of the patented invention. Cf., Titanium Metals Corp. v. Banner, 778 F.2d 775, 227 USPQ 773 (Fed. Cir. 1985) (holding that an earlier species disclosure in the prior art defeats any generic claim) . This court's predecessor has held that, without a terminal disclaimer, the species claims preclude issuance of the generic application. In re Van Ornum, 686 F.2d 937, 944, 214 USPQ 761, 767 (CCPA 1982); Schneller , 397 F.2d at 354. Accordingly, absent a terminal disclaimer, claims 8,14 are properly rejected under the doctrine of obviousness-type double patenting (see In re Goodman (CA FC) 29 USPQ2d 2010).

4. Claim 18 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 35 of U.S. Patent No. 6,647,485. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons :

5. Although the patented claim 35 did not recite making the plurality of instructions available for which the resources were identified as in current claim 18, it would have been obvious to one of ordinary skill in the art to make the plurality of instructions available for which the resources were identified because the patent claim 35 already taught identifying of the execution resources for more than one available instructions (claim 35, col.59, lines 13-15), therefore, one of ordinary skill in the art should be able recognize the use of the identified resources for the available instructions in order to provide the resource for execution , furthermore, claim 18 is generic to the species of invention covered by claim 35 of the patent.

Thus, the generic invention is "anticipated" by the species of the patented invention. Cf., Titanium Metals Corp. v. Banner, 778 F.2d 775, 227 USPQ 773 (Fed. Cir. 1985) (holding that an earlier species disclosure in the prior art defeats any generic claim) . This court's predecessor has held that, without a terminal disclaimer, the species claims preclude issuance of the generic application. In re Van Ornum, 686 F.2d 937, 944, 214 USPQ 761, 767 (CCPA 1982); Schneller , 397 F.2d at 354. Accordingly, absent a terminal disclaimer, claim 18 is properly rejected under the doctrine of obviousness-type double patenting (see In re Goodman (CA FC) 29 USPQ2d 2010).

6. Claims 22,35 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 35 of U.S. Patent No. 6,256,720. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons :

7. Although the patented claim 35 did not the RISC microprocessor as in current claim 22,35, it would have been obvious to one of ordinary skill in the art to include RISC processor as claimed because the patent claim 35 already taught a superscalar microprocessor (claim 35, col.59, lines 3-5), and because no specific type of the RISC processor has been reflected into the current claims 22,35, and because there is no feature in the claim body to support the distinctness of the RISC processor, it is assumed to be any type of superscalar processor, therefore, one of ordinary skill in the art should be able recognize the use of RISC in order to provide the superscalar instruction execution.

8. Claims 22,35 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 5,539,911. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons :

9. Although the patented claim 1 did not teach the RISC microprocessor as in current claim 22,35, the RISC in the preamble is not given patentable weight because there is no feature in the claim body of claims 22,35 to support the distinctness of the RISC processor. Therefore, with this reason, the rest of the claims 22,35 are generic to the species of invention covered by claim 1 of the patent. Thus, the generic invention is "anticipated" by the species of the patented invention. Cf., Titanium Metals Corp. v. Banner, 778 F.2d 775, 227 USPQ 773 (Fed. Cir. 1985) (holding that an earlier species disclosure in the prior art defeats any generic claim) . This court's predecessor has held that, without a terminal disclaimer, the species claims preclude issuance of the generic application. In re Van Ornum, 686 F.2d 937, 944, 214 USPQ 761, 767 (CCPA 1982); Schneller , 397 F.2d at 354. Accordingly, absent a terminal disclaimer, claims 22,35 are properly rejected under the doctrine of obviousness-type double patenting (see In re Goodman (CA FC) 29 USPQ2d 2010).

10. Claims 22,35 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 26 of U.S. Patent No. 6,092,181. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons :

11. Although the patented claim 26 did not teach the RISC microprocessor as in current claim 22,35, it would have been obvious to one of ordinary skill in the art to include RISC processor as claimed because the patent claim 1 already taught a superscalar microprocessor (claim 1, col.57, lines 27-29), and because no specific type of the RISC processor has been reflected into the current claims 22,35, and because there is no feature in the claim body to support the distinctness of the RISC processor, it is assumed to be any type of superscalar processor, therefore, one of ordinary skill in the art should be able recognize the use of RISC in order to provide the enhanced instruction execution

12. Claims 26,39 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 65 of U.S. Patent No. 6,038,654. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons :

13. Although the patented claim 65 did not teach the RISC microprocessor as in current claims 26,39, it would have been obvious to one of ordinary skill in the art to include RISC processor as claimed because the patent claim 65 already taught a superscalar microprocessor (claim 65, col.62, lines 48-51), and because no specific type of the RISC processor has been reflected into the current claims 22,35, and because there is no feature in the claim body to support the distinctness of the RISC processor, the RISC is assumed to be any type of superscalar processor, therefore, one of ordinary skill in the art should be able recognize the applicability of RISC in order to provide the enhanced instruction execution. Furthermore since there is no feature in the current claim body to support the distinctness of the RISC processor, the RISC in the preamble is not given patentable weight , therefore, the rest of the claims 26,39

are generic to the species of invention covered by claim 65 of the patent. Thus, the generic invention is "anticipated" by the species of the patented invention. Cf., Titanium Metals Corp. v. Banner, 778 F.2d 775, 227 USPQ 773 (Fed. Cir. 1985) (holding that an earlier species disclosure in the prior art defeats any generic claim) . This court's predecessor has held that, without a terminal disclaimer, the species claims preclude issuance of the generic application. In re Van Ornum, 686 F.2d 937, 944, 214 USPQ 761, 767 (CCPA 1982); Schneller , 397 F.2d at 354. Accordingly, absent a terminal disclaimer, claims 26,39 are properly rejected under the doctrine of obviousness-type double patenting (see In re Goodman (CA FC) 29 USPQ2d 2010).

14. Claim 31 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 29 of U.S. Patent No. 6,647,485. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons :

15. Although the patented claim 29 did not teach making the instruction concurrently available as in current claim 31, it would have been obvious to one of ordinary skill in the art to make the instruction concurrently available as claimed because the patent claim 31 already taught concurrently identifying the execution resource of available instructions (claim 31, col.58, lines 12-18), therefore, It would have been obvious to one of ordinary skill in the art to recognize the use of the available instructions concurrently for execution based on the concurrently available execution resource(s) in order to increase the processing bandwidth of the superscalar, and therefore, provided a motivation.

16. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vegesna et al. (5,488,729) in view of Hasbrouck et al. (3,718,912) .

17. As to claims 8-12,14-16, 18-20, 31-33, 52 , Vegesna disclosed a superscalar processing system including at least :

a)a fetch circuit [IFETCH] for retrieving a plurality of instructions (see fig.19 [IFETCH], col.22, lines 25-38, col.23, lines 45-50, col.29, lines 6-13, col.30, lines 26-32);

b)an instruction buffer that buffers the plurality of instructions from fetch circuit(see fig.19 [DBUF], col.22, lines 25-38, col.23, lines 45-50, col.29, lines 6-13, col.30, lines 26-32);

c)plurality of functional units (see fig.18 [ALU][FAU][FMU]);

d)register file comprising at least temporary registers for storing execution results (see fig.18, [16][26], col.20, lines 34-67, col.21, lines 1-10, col.24, lines 10-20);

e) bypass control coupled to a plurality of data paths to distribute result of the plurality of functions units and to provide alternate path that bypassed register file (see col.9, lines 18-36).;

d) issuing available instruction concurrently for execution by the functional units (see the simultaneously issuing of the instruction and the independent order of the instructions in col.3, lines 8-38).

18. Vegesna did not specifically show the resource identifying circuit for identifying of the resource as claimed. However, Hasbrouck disclosed a circuit [R field bits] for identifying resource used by instructions (e.g. see the identifying of registers used by instructions execution

in col.4, lines 20-25). It would have been obvious to one of ordinary skill in the art to use Hasbrouck in Vegesna for including the resource identifying circuit as claimed because the use of Hasbrouck could provide the processing ability of Vegesna to a predefined set of registers at a given storage assignment, such as a the identification format of registers , and it could be readily achieved by configuring the identifying bits of Hasbrouck into Vegesna for identifying the resources available for instructions execution in a predetermined sequence, and for the above reasons, provided a motivation.

19. As to claims 9-10,15, 19,32, Vegesna also included floating point and integer functional units (e.g. see fiog.15).

20. As to claims 11,16, 20, Vegesna also included connection to more than one functional unit (see fig.18).

21. AS to claims 12,33, Vegesna also transfer operand data from register file to the functional units (fig.18, [16][26], col.20, lines 34-67, col.21, lines 1-10, col.24, lines 10-20).

22. As to claim 52, Vegesna also included dependencies of the instructions (e.g. see the dependencies col.9, lines 60-67, col.10, lines 1-10).

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the

international application designated the United States and was published under Article 21(2) of such treaty in the English language.

23. Claims 22-26,28-30,35,37-39, 41-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Vegesna et al. (5,488,729).

24. AS to claims 22,26,28,35, 39, 41, Vegesna taught a RISC (see RISC in col. 7, lines 29-35) at least :

)a fetch circuit [IFETCH] for retrieving a plurality of instructions (see fig.19 [IFETCH], col.22, lines 25-38, col.23, lines 45-50, col.29, lines 6-13, col.30, lines 26-32);

b) buffer that buffers the plurality of instructions from fetch circuit(see fig.19 [DBUF], col.22, lines 25-38, col.23, lines 45-50, col.29, lines 6-13, col.30, lines 26-32);

c) execution unit capable of executing comprising a register file [register file] and plurality of functional units (see fig.18 [ALU][FAU][FMU]);

d)register file comprising at least temporary registers for storing execution results (see fig.18, [16][26], col.20, lines 34-67, col.21, lines 1-10, col.24, lines 10-20);

e) dispatching and issuing circuit for simultaneously dispatching instructions (see col.3, lines 50-62);

f) operand routing paths coupled to the register file and the functional units for concurrently transferring operand data (fig.18 , and see fig,.19 for detailed routing);

g) decoder [D] disposed at subsequent stage of buffer [B] for simultaneously decoding plurality of instructions (see the decode stage [D] in fig.15).

25. AS to claim 23, Vegesna also included program order (see col.9, lines 46-50).

26. AS to claims 24, 29,37, 42, Vegesna also included a cache (see the instructions caches in col.7, lines 45-50).

27. AS to claims 25, 30, 38, 43, Vegesna also taught renaming circuit (see col.13, lines 60-64).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

28. Claim 27, 36, 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vegesna in view of Murray (5,142,633) .

29. As to claims 27, 36, 40, Vegesna did not specifically show the retirement circuit for arranging the instruction order as claimed. However, Murray disclosed a system for retiring instruction in program order (e.g. see col.11, lines 9-11, lines 66-68, col.12, lines 1-2). It would have been obvious to one of ordinary kill in the art to use Murray in Vegesna for including the retirement of the instructions as claimed because the use of Murray could provide Vegesna the ability to schedule the instructions execution sequence based on the processing conditions of the instruction , such as the active or inactive status of the instructions, thereby providing issuing

of a predefined order of the instructions , and therefore, minimizing the latency caused by the inactive instructions on the dispatch cycle , in doing so, provided a motivation.

30. Claim 44, 46, 48, 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vegesna et al. (5,488,729) in view of Hasbrouck et al. (3,718,912) as applied to claim 8 above, and further in view of Murray (5,142,633).

31. As to claims 44,46, 48, neither Vegesna nor Hasbrouck specifically show the retirement control logic as claimed . However, Murray disclosed a system for retiring instruction in program order (e.g. see col.11, lines 9-11, lines 66-68, col.12, lines 1-2). It would have been obvious to one of ordinary kill in the art to use Murray in Vegesna for including the retirement of the instructions as claimed because the use of Murray could provide Vegesna the ability to schedule the instructions execution sequence based on the processing conditions of the instruction , such as the active or inactive status of the instructions, thereby providing issuing of a predefined order of the instructions , and therefore, minimizing the latency caused by the inactive instructions on the dispatch cycle , in doing so, provided a motivation.

32. Claims 45, 47, 49 , 51 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new

number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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